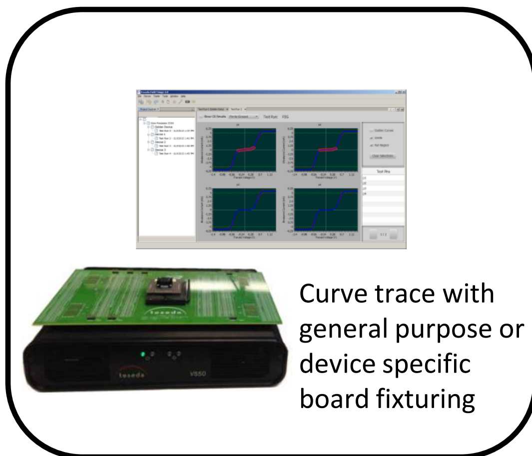
DI Lab System™

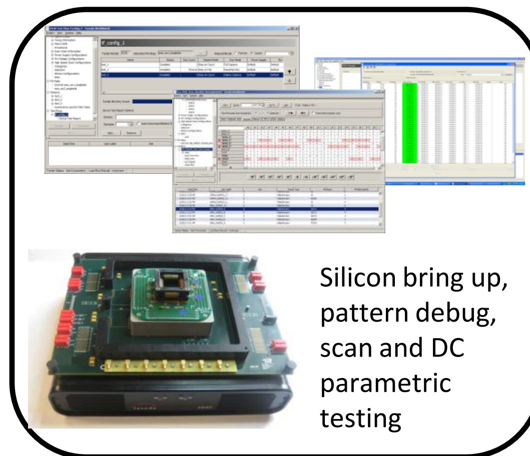
From Silicon Bring Up and Debug to Defect Isolation

DI Lab System™ Highlights:

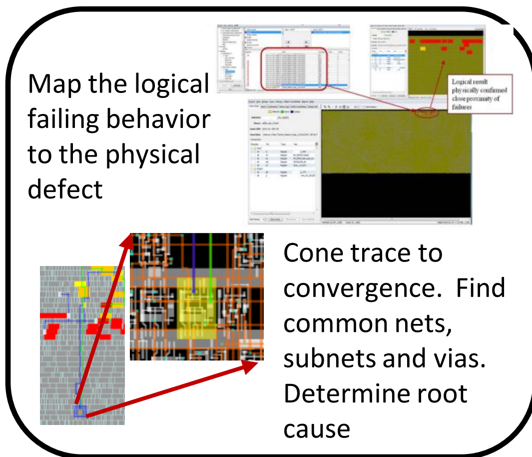
- The **Teseda DI Lab System™** (Defect Isolation), designed from direct user experiences, includes the complete suite of Teseda tools to address the critical needs in device analyses
- Perform continuity, DC parametric testing and curve trace to analyze device current-voltage characteristics
- Automatically detect broken scan chains down to the specific defective scan cell index
- Run the same production tests to understand the logical behavior of failing devices that an ATE cannot provide
- Map failing scan cells against the physical design to localize defects
- Diagnose root cause in one single physical environment



Curve trace with general purpose or device specific board fixturing

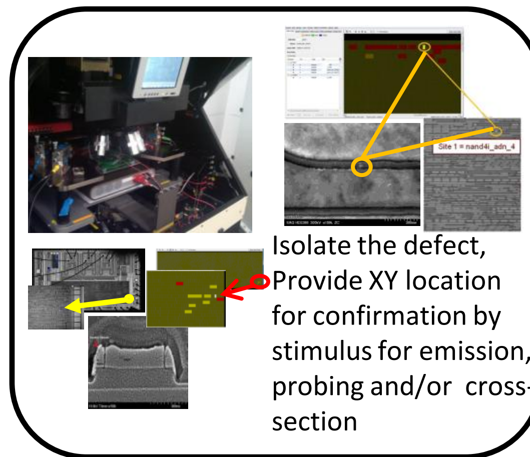


Silicon bring up, pattern debug, scan and DC parametric testing



Map the logical failing behavior to the physical defect

Cone trace to convergence. Find common nets, subnets and vias. Determine root cause



Isolate the defect, Provide XY location for confirmation by stimulus for emission, probing and/or cross-section

Key Benefits:

- Defect isolation in the physical environment in real time independent of costly probabilistic flows
- Work in a single common physical environment, not with a collection of engineering and layout tools
- Rapidly analyze supporting data in physical views as opposed to confusing text reports
- Use and enhance in-house experience to root cause without the need for constant engineering and layout expertise

One system, one environment, one complete diagnostic and test solution

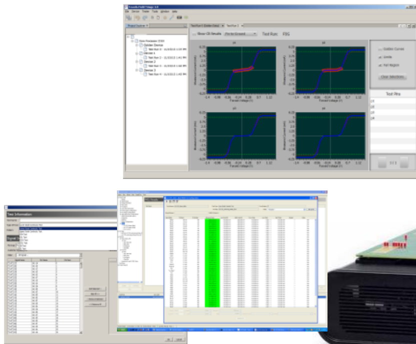
The **Teseda DI Lab System™** is a complete system package of Teseda's patented technology for device test, failure analysis and defect isolation. Finally a solution that keeps all test data and results in one common environment enabling real time diagnostics at the physical level. Teseda links its independent tool sets into one flow enabling the skill set of the user to rationalize resolution of defect behavior, localization and isolation.

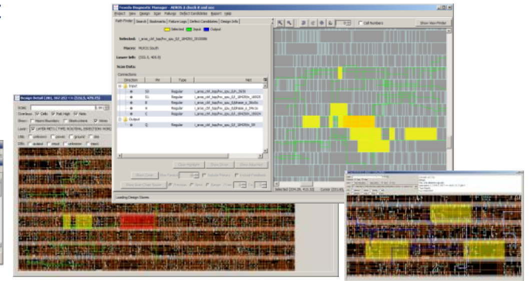
The Teseda flow

Start the flow by determining the electrical characteristics of device pins with curve trace. Make sure of hardware connectivity with the device and that the rest of the hardware configuration has solid contact. Begin your silicon bring up; set the device and pin voltages, import patterns, run the test. Analyze the behavior of failing devices. Map mismatching scan cells against the background of the physical design. Localize the defect area on scan cell mismatch behavior and isolate then isolate the defect through cone tracing and convergence. Whether your discipline is design, test, project or failure analysis engineering, the **Teseda DI Lab System™** offers a complete suite of tools tailored for your respective skill set.

Curve Tracer™
Automated DC Curve Trace

Teseda Workbench ™
Scan-Based Test and Debug, DC Parametric Test





Defect Isolator™
Scan-based Analysis to Localize and Isolate Defects on the Physical Device

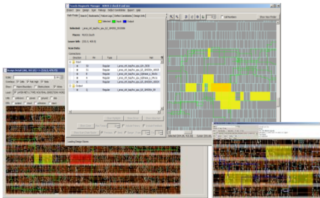
DC Parametric Test
Characterize Force/Measure Current/Voltage

Diagnostic Test Hardware
512 I/O, 100Mhz, 64Mb Pattern Depth

Broken Chain Analyzer™
Identifies Defective Scan Cells in Scan Chains

DI Lab System™

Teseda Defect Isolator™

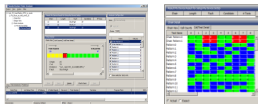


- Highlight mismatching cells to immediately visualize the defect area
- Detailed viewer enables zooming of all physical elements of the design
- Maps fail results to physical location of scan cells, nets, vias, and component internal structures
- Bookmark views of interest consisting of nets, vias and cells
- Patented algorithms for automated cone tracing and convergence provides a unique methodology for defect isolation

Teseda Curve Tracer™

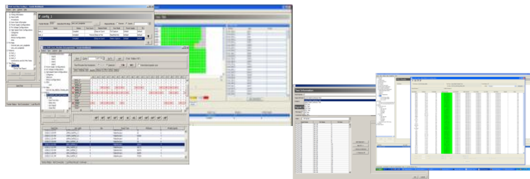
- Test and diagnose Electrical Over-Stress failures
- Identifies failures between IO, power supply and ground pins
- Performs pin-to-ground, pin-to-pin curve trace with overlay
- Retain results for multiple devices

Teseda Broken Chain Analyzer™



- Patented algorithms automatically diagnose captured test failures to isolate defective scan cells in seconds
- Performs diagnosis of captured fail results from scan chain ATPG tests
- No physical probing or laser detection techniques needed

Teseda WorkBench™



DC Parametric Test

- Test control for the Teseda Diagnostic Test Hardware to perform scan-based testing, capture test results in pass/fail, failure capture and full capture modes
- Run single or multiple tests consecutively with pause and looping control features
- Diagnose mismatching scan data to analyze and determine failing trends of behavior
- Specific features to perform connectivity and DC Parametric Test

Teseda Diagnostic Test Hardware™

- 512 I/O, full 100 MHz data rates, 64Mb memory and per-pin timing capabilities
- Built specifically for Scan, Continuity and DC parametric testing
- Seven internal power supplies
  - 4 High Current (4A), 2 Low Current (250mA), 1 High Voltage (25V)
- Runs multiple tests with pause, looping, free running clocks capabilities
- First silicon bring up, device analysis, provides stimulus for dynamic FA applications such as LIVA, TIVA, XIVA, OBIRCH, OBIC, LADA and SEI

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